REMARKS

The Office Action dated on January 14th, 2005 objected claims 12-18 because of informalities and/or defects. The Office Action rejected claims 12-18 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Office Action also rejected claims 12-18 under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art ("AAPA") in view of Li (TW 390013A; May 11, 2000) and/or Ohkawa (US 5,798,560). Applicants have withdrawn claims 1-11 and amended claims 12-18 to further improve the clarity to overcome the objection and the rejection under 35 U.S.C. 112, first paragraph. Applicants have also amended specification to correct the editorial errors and the corrections are supported by the respective drawings (Figs. 2 and 3) of the present invention without introducing further new issues. No new matter has been added to the application by the amendments made herein. After entry of the foregoing amendments, claims 12-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

The Office Action dated on January 14th, 2005 stated that "one of ordinary skill in the art would readily recognize that such triple-well structure is desirable for eliminating the adverse parasitic transistor effect therein and/or reducing leaking current through the substrate, as evidence in Li an/or in Ohkawa". Applicants respectfully disagree.

In the citation, TW 390013A, Li emphasizes that the N-well 22 shown in Fig. 4 is an isolating well for isolating the substrate 20 from the diode elements 24 and 26 respectively (page 10, lines 8-10). It is understood that since the N-well 22 is an isolating well located between the substrate 20 and the diode elements 24 and 26, no parasitic bipolar transistor exists between the P+ doped region 24a, N+ doped region 24b and the substrate 20. However, Li silences about the possible parasitic bipolar diode constructed by the P-well 24, N-well 22 and the substrate 20. Hence, Li neither teach nor suggest to form an extra doped region in the N-well 22 and to establish the relative electrically interconnection between the extra doped region and the diode structure in order to turn off the parasitic bipolar diode.

Further, in citation, U.S. 5,798,560, Ohkawa et al. provide a semiconductor circuit having a spark killing diode. Although Ohkawa et al. mention a diode structure 24 similar to that provided by the present invention and they stated that V_{cc} is equal to or higher than V_A, they do not teach the way to serially connect the diode structures. Ohkawa et al. also fails to suggest that when serially connecting the diode structures 24, only one N-type well region constructed by N+ buried layer 26 and N+ lead regions 41a and 41b is necessary to form in the substrate to enclose all the diode structure in order to decrease the size of the diode string structure.

Moreover, although the Applicants' Admitted Prior Art (AAPA) disclose a semiconductor device similar to the diode string structure of the present invention, the AAPA fails to teach to formed an extra well region to enclose all the string structure to decrease the size of the diode string structure. Neither do AAPA, Li nor Ohkawa et al. teach a way to reduce the

size of the diode string structure. Therefore, even people skilled in the art will not think to modify Li and/or Ohkawa et al. referring to what disclosed in the AAPA to obtain a smaller diode string structure. Applicants respectfully submit that newly amended claim 12 is believed to patentably distinguish over the combination of the prior arts.

CONCLUSION

For at least the foregoing reasons, Applicant respectfully submits that independent claim 12 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 13-18 patently define over the prior art as well. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 4/14/2005

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809